Topic 17 Hardware: Processors – Worksheet

1. Research and Present

a. Draw a diagram of a central processing unit that includes the following components: ALU, general-purpose registers, specialized registers (PC, CIR, MAR, MDR), address bus, and data bus. Show the data connections between the components. **(12)**

b. If the processor above were to have an accumulator register (ACC), where would it be placed? **(1)**

c. Some modern architectures, such as RISC-V do not have an accumulator register (ACC). Explain where the results of a computation are stored in such an architecture. **(1)**

d. In a reduced instruction set architecture, such as ARM or RISC-V, data is copied from memory using a load instruction.

Describe in detail the fetch-decode-execute cycle where the instruction is a load instruction. Assume the address of the data to be loaded is stored in a general-purpose register labelled GP1 and the data loaded is to be stored in a second general-purpose register labelled GP2. Include a description of the contents of the internal CPU registers change during each phase. Include the registers: PC, CIR, MAR, MDR, GP1, and GP2.

Fetch: **(6)**

Decode: **(2)**

Execute: **(3)**